Colophon

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Chapter 1. PCIe connector

The Raspberry Pi 5 is the first Raspberry Pi product to feature a single lane PCI Express (PCIe) connector. This connector is a 16-pin, 0.5mm pitch FFC connector, which is small and low-cost. This document specifies the connector pinout and how to use it if you are developing third-party products.

**IMPORTANT**

The FFC used must be 50mm or shorter, and must offer controlled impedance. See Chapter 3.

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**Figure 1. Raspberry Pi 5 16W PCIe FFC Connector Pinout**

![Diagram of the Raspberry Pi 5 16W PCIe FFC Connector Pinout]

- 5V
- J20
- P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16
- SH1, SH2, SH3, SH4
- 62674-161120ALF
NOTE
Third-party PCIe accessory or adaptor boards are not necessarily constrained to use the HAT form-factor. For instance, they might be mounted underneath the Raspberry Pi. However, unless they obey the HAT specification these boards should not be referred to as HATs.

1.1. Raspberry Pi 5 power states

OFF
No 5V power connected to the board.

WARM-STANDBY
The Raspberry Pi is halted/off but all of the power rails are still enabled – this is the default mode when doing a ‘sudo halt’ or soft power-button-off operation.

STANDBY
The Raspberry Pi has the +5V rail powered (so the PMIC is powered), but no other power supplies on the PMIC/board are enabled. Instead, ‘sudo halt’ or power-button-off can be configured using the EEPROM to enter this mode rather than WARM-STANDBY.

SLEEP
Some rails are off (notably the CPU core), and Linux is in suspend-to-RAM state. Pressing the power button will cause the PMIC to move to the ACTIVE state.

ACTIVE
All rails up and everything running (e.g. running desktop Linux).

NOTE
The SLEEP state is currently untested and unsupported on Raspberry Pi 5.
Chapter 2. Pinout

The Raspberry Pi connector for PCIe has 5V power, ground (GND), and standard single-lane PCIe signals.

The pinout for the vertically mounted FPC connector as used on Raspberry Pi 5 is shown in Figure 2.

The connector carries RX and TX pairs, clock pair, reset, and two GPIOs that are used for both board power enable, wakeup and board detect; as well as power and ground. Please see Figure 1 for the schematic symbol and Figure 2 for the PCB layout of the FFC connector on the Raspberry Pi 5 board.

The SH1-SH3 pins of the 16W FFC (J20) shown in Figure 2 are mechanical mounting pins and are not electrically connected even though we tie them to ground on Raspberry Pi 5.

2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ_N and RST_B sideband signals which operate at 3.3V.

NOTE

On the Raspberry Pi 5 vertical FFC connector shown, the contact fingers are on the right-hand side. The 16-W FFC connector provides 5V power via pins 1 and 2. These pins are each rated at 500mA (for 1A total current).
2.1. PCIe Signals

2.1.1. PCIE_PWR_EN pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. PCIE_DET_WAKE pin

This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus.

Use the PCIe WAKE# to pull this low.
This connector is a 16-pin, 0.5mm pitch FFC connector. The recommended FFC length is 50mm or shorter. The FFC must control the PCIe differential pair impedance to 90Ω±10% over a continuous ground plane.

The FFC must be of the opposite-sides-contact type, see Figure 3. As specified, a same-side-contact PCIe FFC would not be reversible; if inserted the wrong way around it would short the Raspberry Pi 5 and/or the accessory board.
## Appendix A: Release History

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<tr>
<th>Release</th>
<th>Date</th>
<th>Description</th>
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<td>0.7</td>
<td>06 Nov 2023</td>
<td>• Preliminary draft</td>
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<tr>
<td>0.8</td>
<td>16 Nov 2023</td>
<td>• Initial internal release</td>
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<td>0.9</td>
<td>01 Dec 2023</td>
<td>• Internal release</td>
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<tr>
<td></td>
<td></td>
<td>• Changes to FFC specification</td>
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<tr>
<td>1.0</td>
<td>08 Dec 2023</td>
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<tr>
<td>1.1</td>
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