

Raspberry Pi Connector for PCIe

A 16-way PCIe FFC Connector
Specification

Colophon

© 2023-2024 Raspberry Pi Ltd

This documentation is licensed under a Creative Commons [Attribution-NoDerivatives 4.0 International](#) (CC BY-ND).

build-date: 2024-01-15

build-version: 65f6d5c-dirty

Legal disclaimer notice

TECHNICAL AND RELIABILITY DATA FOR RASPBERRY PI PRODUCTS (INCLUDING DATASHEETS) AS MODIFIED FROM TIME TO TIME (“RESOURCES”) ARE PROVIDED BY RASPBERRY PI LTD (“RPL”) “AS IS” AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW IN NO EVENT SHALL RPL BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THE RESOURCES, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

RPL reserves the right to make any enhancements, improvements, corrections or any other modifications to the RESOURCES or any products described in them at any time and without further notice.

The RESOURCES are intended for skilled users with suitable levels of design knowledge. Users are solely responsible for their selection and use of the RESOURCES and any application of the products described in them. User agrees to indemnify and hold RPL harmless against all liabilities, costs, damages or other losses arising out of their use of the RESOURCES.

RPL grants users permission to use the RESOURCES solely in conjunction with the Raspberry Pi products. All other use of the RESOURCES is prohibited. No licence is granted to any other RPL or other third party intellectual property right.

HIGH RISK ACTIVITIES. Raspberry Pi products are not designed, manufactured or intended for use in hazardous environments requiring fail safe performance, such as in the operation of nuclear facilities, aircraft navigation or communication systems, air traffic control, weapons systems or safety-critical applications (including life support systems and other medical devices), in which the failure of the products could lead directly to death, personal injury or severe physical or environmental damage (“High Risk Activities”). RPL specifically disclaims any express or implied warranty of fitness for High Risk Activities and accepts no liability for use or inclusions of Raspberry Pi products in High Risk Activities.

Raspberry Pi products are provided subject to RPL’s [Standard Terms](#). RPL’s provision of the RESOURCES does not expand or otherwise modify RPL’s [Standard Terms](#) including but not limited to the disclaimers and warranties expressed in them.

Table of contents

Colophon	1
Legal disclaimer notice	1
1. PCIe connector	3
1.1. Raspberry Pi 5 power states	4
2. Pinout	5
2.1. PCIe Signals	5
2.1.1. PCIE_PWR_EN pin	6
2.1.2. PCIE_DET_WAKE pin	6
3. FFC	7
Appendix A: Release History	8

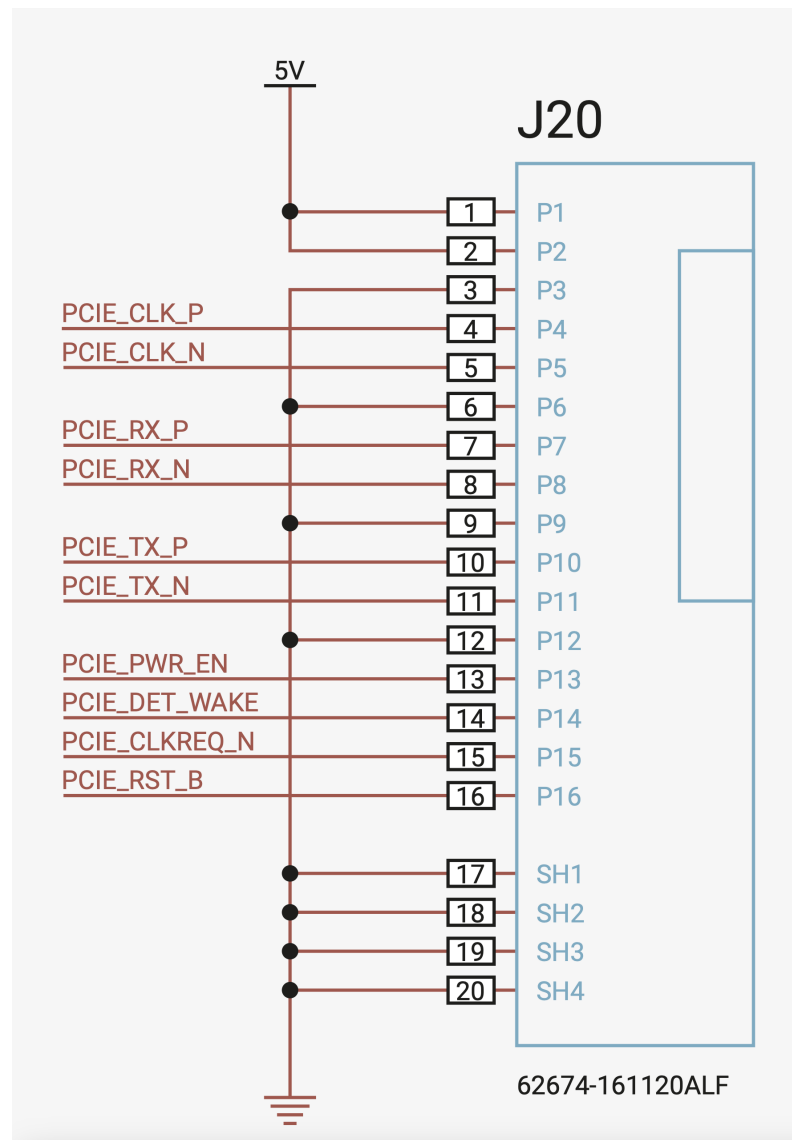
Chapter 1. PCIe connector

The Raspberry Pi 5 is the first Raspberry Pi product to feature a single lane PCI Express (PCIe) connector. This connector is a 16-pin, 0.5mm pitch FFC connector, which is small and low-cost. This document specifies the connector pinout and how to use it if you are developing third-party products.

! IMPORTANT

The FFC used must be 50mm or shorter, and must offer controlled impedance. See [Chapter 3](#).

Figure 1. Raspberry Pi
5 16W PCIe FFC
Connector Pinout



i NOTE

Third-party PCIe accessory or adaptor boards are not necessarily constrained to use the HAT form-factor. For instance, they might be mounted underneath the Raspberry Pi. However, unless they obey the [HAT specification](#) these boards should not be referred to as HATs.

1.1. Raspberry Pi 5 power states

OFF

No 5V power connected to the board.

WARM-STANDBY

The Raspberry Pi is halted/off but all of the power rails are still enabled – this is the default mode when doing a ‘sudo halt’ or soft power-button-off operation.

STANDBY

The Raspberry Pi has the +5V rail powered (so the PMIC is powered), but no other power supplies on the PMIC/board are enabled. Instead, ‘sudo halt’ or power-button-off can be configured using the EEPROM to enter this mode rather than **WARM-STANDBY**.

SLEEP

Some rails are off (notably the CPU core), and Linux is in suspend-to-RAM state. Pressing the power button will cause the PMIC to move to the **ACTIVE** state.

ACTIVE

All rails up and everything running (e.g. running desktop Linux).

i NOTE

The **SLEEP** state is currently untested and unsupported on Raspberry Pi 5.

Chapter 2. Pinout

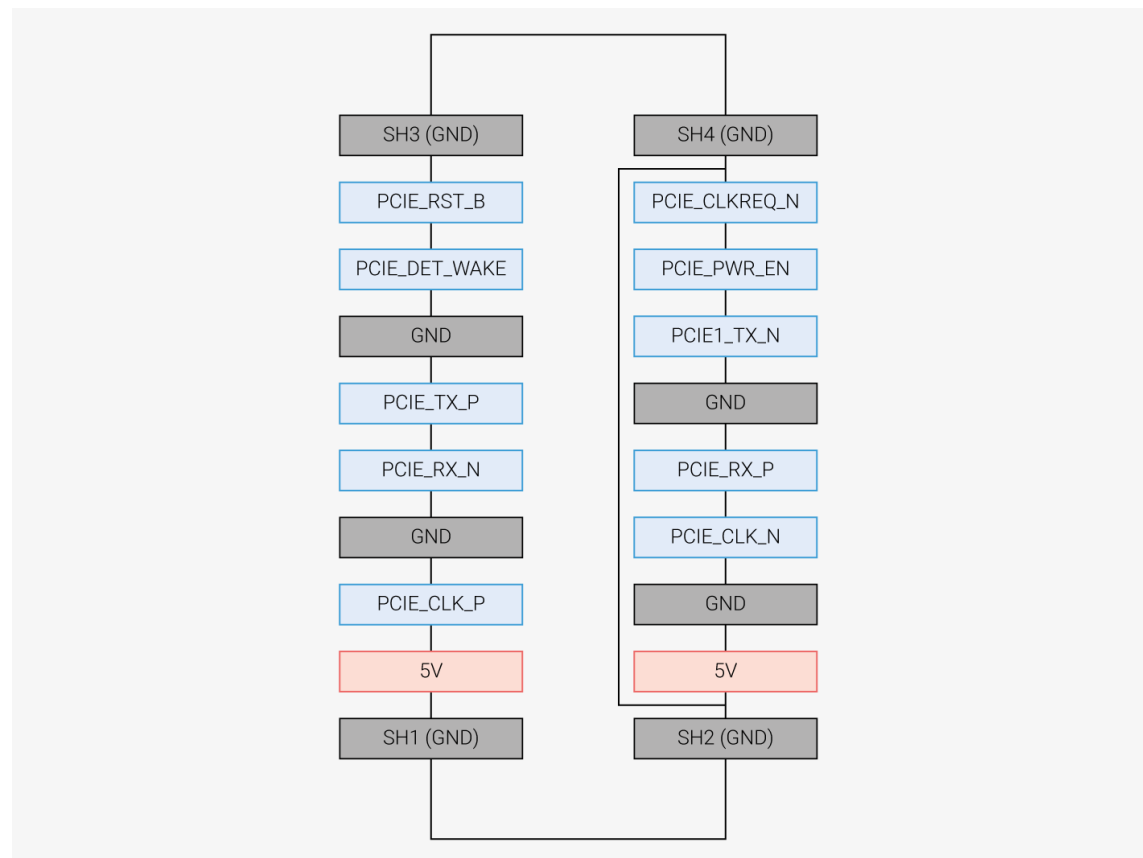
The Raspberry Pi connector for PCIe has 5V power, ground (GND), and standard single-lane PCIe signals.

The pinout for the vertically mounted FPC connector as used on Raspberry Pi 5 is shown in [Figure 2](#).

The connector carries RX and TX pairs, clock pair, reset, and two GPIOs that are used for both board power enable, wakeup and board detect; as well as power and ground. Please see [Figure 1](#) for the schematic symbol and [Figure 2](#) for the PCB layout of the FFC connector on the Raspberry Pi 5 board.

The SH1-SH3 pins of the 16W FFC (J20) shown in [Figure 2](#) are mechanical mounting pins and are not electrically connected even though we tie them to ground on Raspberry Pi 5.

Figure 2. Vertical FFC footprint on Raspberry Pi 5 (FFC contact fingers on RHS)



i NOTE

On the Raspberry Pi 5 vertical FFC connector shown, the contact fingers are on the right-hand side. The 16-W FFC connector provides 5V power via pins 1 and 2. These pins are each rated at 500mA (for 1A total current).

2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ_N and RST_B sideband signals which operate at 3.3V.

i NOTE

Signals can be run at Gen 3 speeds, but this is not officially supported.

2.1.1. PCIE_PWR_EN pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. PCIE_DET_WAKE pin

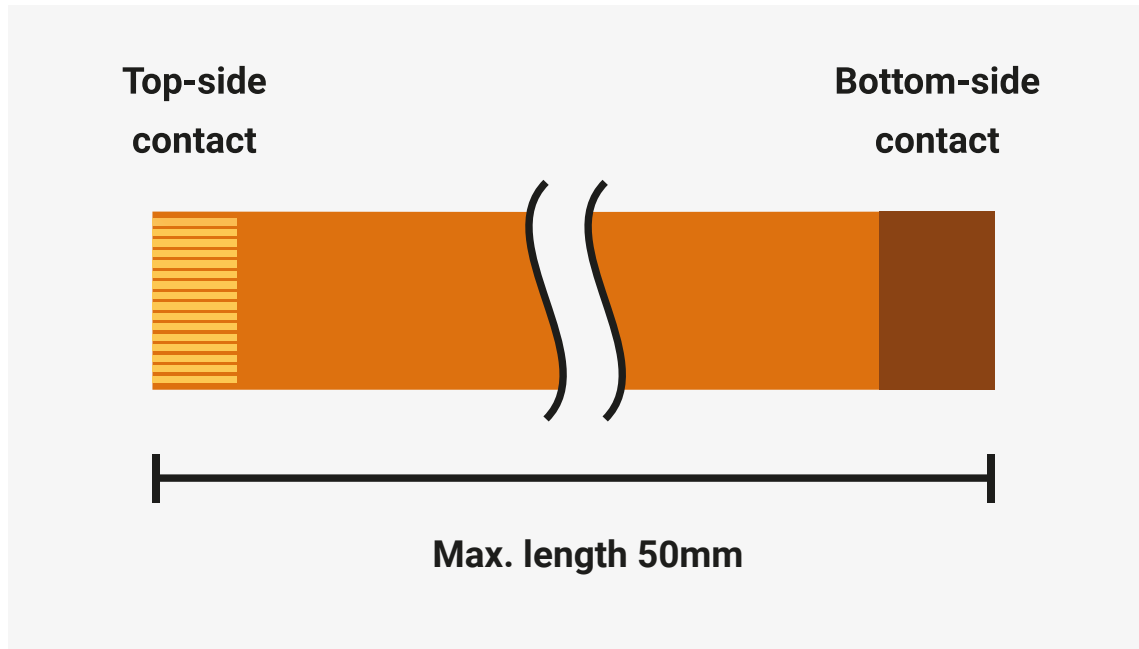
This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus.

Use the PCIe **WAKE#** to pull this low.

Chapter 3. FFC

This connector is a 16-pin, 0.5mm pitch FFC connector. The recommended FFC length is 50mm or shorter. The FFC must control the PCIe differential pair impedance to $90R \pm 10\%$ over a continuous ground plane.

Figure 3. The FFC



The FFC **must** be of the opposite-sides-contact type, see [Figure 3](#). As specified, a same-side-contact PCIe FFC would not be reversible; if inserted the wrong way around it would short the Raspberry Pi 5 and/or the accessory board.

Appendix A: Release History

Table 1.
Documentation
release history

Release	Date	Description
0.7	06 Nov 2023	<ul style="list-style-type: none">• Preliminary draft
0.8	16 Nov 2023	<ul style="list-style-type: none">• Initial internal release
0.9	01 Dec 2023	<ul style="list-style-type: none">• Internal release• Changes to FFC specification
1.0	08 Dec 2023	<ul style="list-style-type: none">• Public release
1.1	15 Jan 2024	<ul style="list-style-type: none">• Minor updates



Raspberry Pi is a trademark of Raspberry Pi Ltd